Code No: **R41021** **R10** **Set No. 1**

IV B.Tech I Semester Regular/Supplementary Examinations, Nov/Dec - 2015

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1 a) Convert i) $(3A6.D87)_{16}$ to Octal ii) $(324)_{10}$ to Binary and Hexadecimal [6]

b) Briefly explain about IEEE floating point representation and perform addition of two floating numbers. [9]

2 a) Draw the bus system for four registers using tri-state buffer and decoder and explain. [7]

b) Describe about logical and shift microoperations with suitable applications. [8]

3 a) Draw the flowchart for memory reference instructions and explain. [8]

b) Discuss about stack organization with register stack and memory stack. [7]

4 a) Draw the micro program sequencer for a control memory and explain. [8]

b) Explain the difference between hardwired control and micro programmed control. Is it possible to have a hardwired control associated with a control memory? Justify. [7]

5 a) Explain the procedure for converting the logical address into physical address with an example. [8]

b) Discuss about memory hierarchy in a computer system in detail. [7]

6 a) Differentiate between isolated Vs memory mapped I/O. [7]

b) Briefly explain the asynchronous serial transfer with an example. [8]

7 a) How to handle the branch instructions in instruction pipeling and explain [8]

b) Write about the SIMD array processor organization. [7]

8 Write short notes on any Two

a) Characteristics of RISC

b) Any one Mapping method for cache memory

c) Design of One stage ALU [15]

Code No: **R41021** **R10** **Set No. 2**

IV B.Tech I Semester Regular/Supplementary Examinations, Nov/Dec - 2015

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1 a) Convert i) $(364.277)_8$ to Hexadecimal ii) $(124)_{10}$ to Binary and Octal [8]

b) Draw the basic computer system and explain each block in detail. [7]

2 a) Design a combinational circuit for [8]
i) 4-bit adder-subtractor ii) 4-bit incrementer- decrementer and explain.

b) Draw the flowchart for instruction cycle with necessary control functions and microoperations. [7]

3 a) An instruction is stored at location 300 with its address field at location 301. The address filed has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is i) direct ii) immediate iii) relative iv) register indirect v) index with R1 as the index register [8]

b) Briefly explain the program control instructions with an example. [7]

4 a) Draw the block diagram for micro programmed control organization and explain. [8]

b) Explain the procedure for selection of address for control memory with help of diagram. [7]

5 a) Explain about the Set-associate mapping procedure for cache memory. [8]

b) Discuss about the operation principle of magnetic disks and magnetic tapes. [7]

6 a) Briefly explain the Daisy-chain priority interrupt with the help of block diagram. [8]

b) Draw the block diagram of DMA transfer in a computer system and explain. [7]

7 a) Explain about Flynn's classification of computers for parallel processing [7]

b) Discuss about the major difficulties that cause the instruction pipeline to deviate from its normal operation [8]

8 Write short notes on any Two

a) Design of Arithmetic circuit (add, sub, inc, dec) using 2X1 mux and adders

b) Virtual Memory

c) Memory reference instructions [15]

Code No: **R41021** **R10** **Set No. 3**

IV B.Tech I Semester Regular/Supplementary Examinations, Nov/Dec - 2015

COMPUTER ORGANIZATION

(Electrical and Electronics Engineering)

Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions
All Questions carry equal marks
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1 a) Discuss about the computer types with suitable examples [8]

b) Briefly explain about fixed point representation and perform multiplication of two fixed point numbers [7]

2 a) Design a combinational circuit for i) 4-bit shifter ii) 4-bit decrementer and explain. [8]

b) Briefly explain the computer registers for basic computer. [7]

3 a) Briefly explain the data manipulation instructions with an example [8]

b) The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two-word call subroutine is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP and the top of the stack:
i) Before the call instruction is fetched from memory?
ii) After the call instruction is executed?
iii) After the return from subroutine? [7]

4 a) Formulate a mapping procedure that provides eight consecutive microinstructions for each routine. The operation code has six bits and the control memory has 2048 words [6]

b) Explain the concept of address sequencing for control memory. [9]

5 a) Discuss about the direct mapping procedure for cache memory. [8]

b) An address space is specified by 24 bits and the corresponding memory space by 16 bits.
i) How many words are there in the address space?
ii) How many words are there in the memory space?
iii) If a page consists of 2K words, how many pages and blocks are there in the system? [7]

6 a) Draw the block diagram of a typical asynchronous communication interface and explain. [8]

b) Draw the block diagram of DMA control and explain. [7]

7 a) Explain the vector processing with suitable applications. [8]

b) With an example explain about arithmetic pipeline. [7]

8 Write short notes on any Two
a) RISC pipeline b) Microprogram Sequencer c) Instruction formats [15]

Code No: **R41021** **R10** **Set No. 4**

IV B.Tech I Semester Regular/Supplementary Examinations, Nov/Dec - 2015

COMPUTER ORGANIZATION

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Time: 3 hours **Max. Marks: 75**

Answer any FIVE Questions

All Questions carry equal marks

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1 a) Explain the multiplication and division of two floating point numbers by using flowchart. [8]

b) Convert (i) $(24.125)_{10}$ to Hexadecimal (ii) $(D6E4)_{16}$ to Binary and Octal [7]

2 a) Design a combinational circuit for the following arithmetic operations
(i) Addition (ii) Subtraction (iii) Increment (iv) decrement. [8]

b) Discuss about instruction codes and stored program organization. [7]

3 a) Write the major characteristics of RISC and explain [7]

b) Write a program to evaluate the arithmetic expression
X = A – B + C *(D*E-F)/G + H * Using a general register computer with i) three-address instructions ii) Two-address instructions
iii) one-address instructions iv) zero-address instructions [8]

4 a) Briefly explain the design of control unit with necessary diagrams. [8]

b) Explain how the mapping from an instruction code to a microinstruction address can be done by means of a read only memory. [7]

5 a) Write about the concept of virtual memory with an example. [10]

b) A two-way set associative cache memory uses blocks of four words.The cache can accommodate a total of 2048 words fro main memory. The main memory size is 128K X 32
i) Formulate all pertinent information required to construct the cache memory.
ii) What is the size of the cache memory? [5]

6 a) Discus about asynchronous data transfer using strobe control and handshaking. [8]

b) Write about programmed I/O with an example. [7]

7 a) Discuss about instruction pipeline with timing diagram [8]

b) Explain about memory interleaving concept in vector processing [7]

8 Write short notes on any Two
a) Design of 4-bit shifter and incrementer-decrementer
b) Priority Interrupt
c) Flow chart for instruction cycle

[15]